

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
*( Not for submission under 37 CFR 1.99)*

Application Number	09989777
Filing Date	2001-11-19
First Named Inventor	Craig Nemecek
Art Unit	2123
Examiner Name	Mary C. Jacob
Attorney Docket Number	CD01208M

**U.S.PATENTS**

Examiner Initial*	Cite No	Patent Number	Kind Code <sup>†</sup>	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	6636096	B1	2003-10-21	Schaffer et al.	Entire Document
	2	6560306	B1	2003-05-06	Duffy et al.	Entire Document
	3	6680632	B1	2004-01-20	Meyers et al.	Entire Document
	4	6683930	B1	2004-01-27	Dalmia	Entire Document
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	6	6782068	B1	2004-08-24	Wilson et al.	Entire Document
	7	7138868	B1	2006-11-21	Sanchez et al.	Entire Document
	8	6686787	B1	2004-02-03	Ling, Kuok	Entire Document

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9	6617888	B1	2003-09-09	Volk, Andrew M.	Entire Document
10	6597212	B1	2003-07-22	Wang et al.	Entire Document
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34	6380811	B1	2002-04-30	Zarubinsky et al.	Entire Document
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**U.S. PATENT APPLICATION PUBLICATIONS**

Examiner Initial*	Cite No	Publication Number	Kind Code†	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20050280453	A1	2005-12-22	Hsieh	Entire Document

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**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No	Foreign Document Number <sup>3</sup>	Country Code <sup>2</sup> i	Kind Code <sup>4</sup>	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T <sup>5</sup>
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**NON-PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>5</sup>
	1	Application Number 10/226,911 (CD02112): "Calibration of Integrated Circuit Time Constants," Gehring et al., 32 pages 8/22/02	<input type="checkbox"/>
	2	USPTO Notice of Allowance for Application Number 09/943,149 (CD01085) dated 01/12/2004, 7 pages	<input type="checkbox"/>
	3	USPTO Non-Final Rejection for Application Number 09/943,149 (CD01085) dated 08/28/2003, 9 pages	<input type="checkbox"/>
	4	USPTO Final Rejection for Application Number 09/943,149 (CD01085) dated 05/07/2003; 10 pages	<input type="checkbox"/>
	5	USPTO Non-Final Rejection for Application Number 09/943,149 (CD01085) dated 11/20/2002; 7 pages	<input type="checkbox"/>
	6	Application Number 09/943,149 (CD01085): "Method for Phase Locking in a Phase Lock Loop," Moyal et al.; 21 pages 8/30/01	<input type="checkbox"/>
	7	Durham et al., "Integrated Continuous-Time Balanced Filters for 16-bit DSP Interfaces," IEEE, 1993; 6 pages	<input type="checkbox"/>

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8	Durham et al., "Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering," IEEE, 1992; 7 pages	<input type="checkbox"/>
9	Durham et al., "High-Linearity Continuous-Time Filter in 5-V VLSI CMOS," IEEE, 1992; 8 pages	<input type="checkbox"/>
10	Application Number 09/047,595 (CD97115): "Roving Range Control to Limit Receive PLL Frequency of Operation," Scott; 35 pages <b>3/25/98</b>	<input type="checkbox"/>
11	Application Number 09/216,460 (CD98099): "Circuit and Method for Controlling an Output of a Ring Oscillator," Abugharbieh et al.; 21 pages <b>12/18/98</b>	<input type="checkbox"/>
12	Application Number 09/471,914 (CD99064): "Reference-Free Clock Generator and Data Recovery PLL," Dalmia et al.; 32 pages <b>12/23/99</b>	<input type="checkbox"/>
13	Application Number 09/471,576 (CD99062): "Reference-Free Clock Generation and Data Recovery PLL," Dalmia; 30 pages <b>12/23/99</b>	<input type="checkbox"/>
14	Application Number 10/063,442 (CD01264): "Method/Architecture for a Low Gain PLL with Wide Frequency Range," Meyers et al.; 28 pages <b>2/26/02</b>	<input type="checkbox"/>
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18	Application Number 09/398,956 (CD99049): "Frequency Acquisition Rate Control in Phase Lock Loop Circuits," Moyal et al.; 35 pages <b>9/17/99</b>	<input type="checkbox"/>

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19	Application Number 09/747,262 (CD00085): "Linearized Digital Phase-Locked Loop," Williams et al.; 9 pages <b>12/22/00</b>	<input type="checkbox"/>
20	Application Number 09/981,448 (CD01102): "Oscillator Tuning Method," Hauck; 28 pages <b>10/17/01</b>	<input type="checkbox"/>
21	Application Number 09/538,989 (CD98104): "Memory Based Phase Locked Loop," Krishnan; 27 pages <b>3/30/00</b>	<input type="checkbox"/>
22	Application Number 09/048,905 (CD95045): "Programmable Clock Generator," Mann et al., 42 pages <b>3/26/98</b>	<input type="checkbox"/>
23	Application Number 08/865,342 (CD95045C): "Programmable Clock Generator," Mann et al., 41 pages <b>5/29/97</b>	<input type="checkbox"/>
24	USPTO Notice of Allowance for Application Number 10/293,392 (CD02135) dated 03/10/2004; 6 pages	<input type="checkbox"/>
25	USPTO Non-Final Rejection for Application Number 10/293,392 (CD02135) dated 10/16/2003; 6 pages	<input type="checkbox"/>
26	Application Number 10/293,392 (CD02135): "Low Voltage Receiver Circuit and Method for Shifting the Differential Input Signals of the Receiver Depending on a Common Mode Voltage of the Input Signals," Maher et al.; 20 pages <b>11/13/02</b>	<input type="checkbox"/>
27	USPTO Notice of Allowance for Application Number 10/288,003 (CD02108) dated 01/14/2005; 6 pages	<input type="checkbox"/>
28	USPTO Final Rejection for Application Number 10/288,003 (CD02108) dated 10/06/2004; 6 pages	<input type="checkbox"/>
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11/4/02



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**EXAMINER SIGNATURE**

Examiner Signature /Mary Jacob/ Date Considered 07/29/2009

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> See Kind Codes of USPTO Patent Documents at [www.USPTO.GOV](http://www.USPTO.GOV) or MPEP 901.04. <sup>2</sup> Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>3</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>4</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST 16 if possible. <sup>5</sup> Applicant is to place a check mark here if English language translation is attached.

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